

REMARKS

Claims 1-30 have been examined. The Examiner has indicated that claims 7-10 and 17-20 would be allowable if rewritten in independent form. Applicant is amending the specification to correct a typographical error and adding new claims 31-35. Claims 1-35 are all the claims pending in the application.

Applicant thanks the Examiner for acknowledging Applicant's claim to foreign priority under 35 U.S.C. § 119(a) - (d) and further for acknowledging receipt of all certified copies of the priority documents. Applicant also thanks the Examiner for accepting the formal drawings filed on February 8, 1999.

Applicant thanks the Examiner for considering all the references cited in Applicant's Information Disclosure Statement (hereinafter IDS) filed on February 4, 2002. However, Applicant respectfully requests that the Examiner consider, by the next Office communication, the references cited in Applicant's IDS filed on February 20, 2002.

This Amendment is believed to be fully responsive to each point of objection and rejection raised by the Examiner in the non-final Office action dated August 1, 2002. Accordingly, Applicant respectfully requests favorable reconsideration and allowance of the pending claims.

Objection to the Specification

The Examiner has objected to the abstract of the disclosure because numbers recited

therein are not in parentheses. Applicant reviewed MPEP §608.01(b)(Abstract of the Disclosure)(8th Edition) and found no requirement that numbers be in parentheses, as alleged by the Examiner. Therefore, Applicant has not amended the abstract of the disclosure and respectfully requests that the objection to the abstract of the disclosure under MPEP §608.01(b), be withdrawn.

Rejection of Claims 1-4, 11-14, 21-24, 26-28 and 30 under 35 U.S.C. § 102(e) - Miller

The Examiner has rejected claims 1-4, 11-14, 21-24, 26-28 and 30 under 35 U.S.C. § 102(e) as allegedly being anticipated by U.S. Patent No. 5,731,823 (hereinafter Miller). Applicant respectfully traverses this rejection.

Miller describes that photograph regions 48 are processed at step 108. (See column 8, line 54 through column 9, line 26). At step 104, halftone parameters are controlled based upon second characterization data 100, and the allegedly corresponding half-toning step 68 halftones the resulting resolution specific image for a specific pixel image. (Figure 3B). The business graphics 46 may be halftoned with a different technique than scanned photographs 48. (Column 9, lines 28-37).

The Examiner alleges that the photograph region (allegedly corresponding to high-resolution raster data) and the graph region (allegedly corresponding to low-resolution raster data) are halftoned by different techniques, and that the photograph region that is processed at step 108, separate from step 68, is applicable to the claimed invention.

However, Miller does not clearly disclose that an image of high-resolution data is converted into that of low-resolution data, and a second image element is low-resolution data. In other words, Miller fails to disclose that the data such as graphics have been halftoned in advance, in the allegedly corresponding upper apparatus.

In contrast, with respect to claim 1, it is understood that second image data has been halftoned before being sent to the claimed image completion circuit. Therefore, Miller fails to disclose the claimed low-resolution raster data for a second image element.

Additionally, the Examiner alleges that step 75 of Figure 3B of Miller corresponds and anticipates the image completion circuit. However, this assertion is incorrect for the following reasons.

The claimed image completion circuit employs second low-resolution data, for a second image element, that is transmitted from an upper apparatus. The Examiner alleges that column 9, lines 25-40 of Miller anticipates this aspect of the image completion circuit. However, Miller fails to describe an upper apparatus transmitting low-resolution data for a second image. Rather, column 7, line 58 through column 8, line 5 of Miller describes that the rasterization controlling step 88 may rasterize textual and graphic 45, 46, to a lower resolution.

While column 4, lines 42-67 of Miller, describes that the steps of flow chart 50 may occur in the host computer or in the printer hardware, or in any combination of these locations, Miller fails to specifically disclose the above-mentioned limitation.

Under MPEP §2131(8th Edition), a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. Verdegaal Bros. V. Union Oil Co. of California, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Also, the identical invention must be shown in as complete detail as is contained in the claim. Based on the identified deficiencies of Miller, the Examiner has failed to support a rejection under 35 U.S.C. § 102(e) because all the claim limitations are not taught by the prior art. MPEP §2131 (8th Edition).

For at least these reasons, Applicant respectfully requests that the rejection of independent claim 1 and dependent claims 2-4 under 35 U.S.C. § 102(e) be withdrawn.

Since independent claims 11, 21, 26 and 30 contain features that are similar to the features discussed above in conjunction with independent claim 1, then claims 11-14, 21-24, 26-28 and 30 are patentable for at least the reasons presented above.

Rejection of Claims 5, 6, 15, 16, 25 under 35 U.S.C. § 103(a) - Miller and Schoon

The Examiner has rejected claims 5, 6, 15, 16 and 25 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Miller as applied to claims 1, 11 and 21 above, and further in view of U.S. Patent No. 4,857,904 (hereinafter Schoon). Applicant respectfully traverses this rejection.

Applicant notes that Miller and Schoon, individually or in combination, fail to teach or suggest independent claims 1, 11 and 21. Therefore, claims 5-6, 15-16 and 25 are patentable at

least by virtue of their dependency. Applicant also provides the following supplemental comments.

With respect to claims 5, 15 and 25, Figure 3b, printing step 75 of Miller and column 10, lines 25-35 of Schoon, fail to render obvious superimposing first and second raster data into memory. Indeed, Miller and Schoon fail to teach or suggest storing the print information in the manner claimed by Applicant.

Indisputably, Miller fails to even mention storing raster data and while printing step 75 apparently relates to the printing of raster data, the Examiner has read limitations into Miller that do not exist.

Additionally, Schoon apparently describes either a bit-mapped RAM for representing black and white or parallel RAMS (RAM 1 and RAM 2) for representing respective transitions from white to black or from black to white. In contrast, Applicant's claimed superimposing for managing and storing raster data relating to first and second image elements are not suggested by Schoon, where "1" represents black and "0" represents white.

For at least these reasons, the rejection of claims 5-6, 15-16 and 25 under 35 U.S.C. § 103(a) should be withdrawn.

Rejection of Claim 29 under 35 U.S.C. § 103(a) - Miller and Furuya

The Examiner has rejected claim 29 under 35 U.S.C. § 103(a) as allegedly being

unpatentable over Miller as applied to claim 26, and further in view of U.S. Patent No. 6,304,335 (hereinafter Furuya). Applicant respectfully traverses this rejection.

Applicant notes that Miller and Furuya, individually or in combination, fail to teach or suggest independent claim 26. Therefore, claim 29 is patentable at least by virtue of its dependency. Applicant also provides the following supplemental comments.

The Examiner alleges that column 7, lines 5-20 and column 8, lines 1-10 of Furuya teach or suggest the claimed transmitting a raster end command when a first or second image element is not available. However, the block start commands 32 or job end command 34 of Furuya fail to teach, suggest, or correspond to the claimed transmitting a raster end command for instructing raster termination of a pertinent image element when a first or second image element is not available. Furuya is silent as to this aspect of Applicant's invention.

Additionally, the Examiner's reasons to modify Miller are not found in the prior art and stem from impermissible hindsight.

Claims 7-10 and 17-20

Applicant has chosen not to rewrite claims 7-10 and 17-20 in independent form because the prior art, relied on by the Examiner, fails to anticipate or render obvious the respective base claims. Therefore, claims 7-10 and 17-20 should be patentable at least by virtue of their dependency.

New Claims

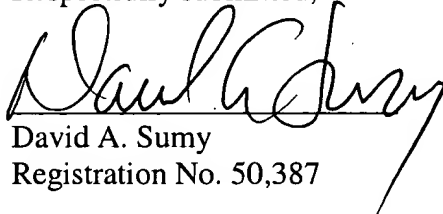
New claims 31-35 should be patentable at least by virtue of their dependency.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,


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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The specification is changed as follows:

Page 16, first full paragraph:

The selector 105 is connected to four head address registers 93 to 99 in which the head addresses for the C, M, Y and K planes 111C to 111K are held. Upon receiving a color selection signal from the color selection counter 101, the selector 105 selects one of the four head address registers 93 to 99, and reads the head address from the selected head address register and outputs it. A synthesization circuit 107 generates a write address by combining the color plane head address received from the selector 105, the vertical address received from the vertical address counter 91 and the horizontal address received from the horizontal address counter 103, and registers it in a write address register 109. The write address that is registered in the write address register 109 is transmitted to the memory control circuit 19. The memory control circuit ~~109~~19 writes, at the write address in the memory 21, the write data that are received from the raster data processing circuits 83 to 85 in Fig. 5. This writing process is effected by using new data to OR the data that are already present at the address.

IN THE CLAIMS:

Claims 31-35 are added as new claims.